AMENDMENTS TO THE CLAIMS

Please replace all prior versions of the claims with the following claim listing:

Claims:

1-26. (Canceled)

27. (Previously Presented) A method comprising:

starting a boundary scan test;

transitioning a Test Access Port (TAP) controller when a ground bounce occurs during the boundary scan test, the TAP controller being transitioned from any of at least three undetermined controller states to a determined controller state, whereby transitioning the TAP controller to a determined controller state recovers the TAP controller from the ground bounce during the boundary scan test; and

resuming the boundary scan test when the TAP controller has been recovered from the ground bounce.

28. (Previously Presented) The method recited in claim 27, wherein the at least three undetermined controller states are selected from the group consisting of an UPDATE state, a RUN-TEST/IDLE state, a SELECT-DR-SCAN state, and a CAPTURE-DR state.

29. (Previously Presented) The method recited in claim 28, wherein the at least three undetermined controller states include an UPDATE state, a RUN-TEST/IDLE state, and a SELECT-DR-SCAN state.

30. (Previously Presented) The method recited in claim 27, wherein the determined controller state is an UPDATE-DR state.

31. (Previously Presented) The method recited in claim 27, wherein the at least three undetermined controller states include an UPDATE state, a RUN-TEST/IDLE state, a SELECT-DR-SCAN state, and a CAPTURE-DR state.

32. (Previously Presented) The method recited in claim 27, wherein transitioning the TAP controller further comprises:

providing a low Test Mode Select input to the TAP controller prior to a falling edge of a clock signal while in an UPDATE state.

33. (Previously Presented) The method recited in claim 32, wherein transitioning the TAP controller further comprises:

providing the TAP controller with a Test Mode Select input having the following bit pattern for a consecutive series of rising edges of clock signals: a plurality of lows, high, a plurality of lows, high, high.

34. (Previously Presented) The method recited in claim 32, wherein transitioning the TAP controller further comprises:

providing the TAP controller with a Test Mode Select input having the following bit pattern for a consecutive series of rising edges of clock signals: low, high, low, high, high.

35. (Previously Presented) An apparatus for conducting a boundary scan test, the apparatus comprising:

at least one Test Access Port (TAP) controller; and

means for transitioning the TAP controller when a ground bounce occurs during a boundary scan test, the transitioning means configured to transition the TAP controller from any of at least three undetermined controller states to a determined controller state to recover the TAP controller from the ground bounce, thereby allowing the boundary scan test to resume when the TAP controller is recovered from the ground bounce.

36. (Previously Presented) The apparatus recited in claim 35, wherein the transitioning means further comprises:

means for providing the TAP controller with a low Test Mode Select input prior to a falling edge of a clock signal while in an update state.

37. (Previously Presented) The apparatus recited in claim 36, wherein the determined controller state is an UPDATE-DR state.

38. (Previously Presented) The apparatus recited in claim 37, wherein the at least three undetermined controller states are selected from the group consisting of an UPDATE state, a RUN-TEST/IDLE state, a SELECT-DR-SCAN state, and a CAPTURE-DR state.

39. (Previously Presented) The apparatus recited in claim 38, wherein the at least three undetermined controller states include an UPDATE state, a RUN-TEST/IDLE state, and SELECT-DR-SCAN state.

40. (Previously Presented) The apparatus recited in claim 39, wherein the transitioning means further comprises:

means for providing the TAP controller with a Test Mode Select input having the following bit pattern for consecutive series of rising edges of clock signals: low, high, low, high, high.

41. (Previously Presented) The apparatus recited in claim 38, wherein the at least three undetermined controller states include an UPDATE state, a RUN-TEST/IDLE state, a SELECT-DR-SCAN state, and a CAPTURE-DR state.

42. (Previously Presented) The apparatus recited in claim 41, wherein the transitioning means further comprises:

means for providing the TAP controller with a Test Mode Select input having the following bit pattern for a consecutive series of rising edges of clock signals: a plurality of lows, high, a plurality of lows, high, high.

43. (Currently Amended) A testing circuit comprising:

~~a first circuit~~ first logic configured to provide a Test Access Port (TAP) controller with a low Test Mode Select input prior to a transition from an update state; and

~~a second circuit~~ second logic configured to transition the TAP controller when a ground bounce occurs during a boundary scan test, the second ~~circuit~~ logic transitioning the TAP controller from any of at least four undetermined controller states to a determined controller state to thereby recover the TAP controller from the ground bounce during the boundary scan test;

wherein the boundary scan test can be resumed when the TAP controller has been recovered from the ground bounce.

44. (Currently Amended) The ~~apparatus~~ testing circuit recited in claim 43, wherein the first ~~circuit~~ logic is further configured to provided the TAP controller with a Test Mode Select input having the following bit pattern for a consecutive series of rising edges of clock signals: a plurality of lows, high, a plurality of lows, high, high.

45. (Currently Amended) The ~~apparatus~~ testing circuit recited in claim 43, wherein the TAP controller is one of a plurality of controllers in a boundary scan chain.

46. (Currently Amended) The ~~apparatus~~ testing circuit recited in claim 43, wherein the at least four undetermined controller states include an UPDATE state, a RUN-TEST/IDLE state, a SELECT-DR-SCAN state, and a CAPTURE-DR state.

47. (Currently Amended) The ~~apparatus~~ testing circuit recited in claim 46, wherein the first ~~circuit~~ logic is further configured to provided the TAP controller with a Test Mode Select input having the following bit pattern for a consecutive series of rising edges of clock signals: a plurality of lows, high, a plurality of lows, high, high.

48. (Currently Amended) The ~~apparatus~~ testing circuit recited in claim 47, wherein the TAP controller is one of a plurality of controllers in a boundary scan chain.

49. (Currently Amended) The ~~apparatus~~ testing circuit recited in claim 43, wherein the second ~~circuit~~ logic is further configured to operationally transition the TAP controller from an undetermined data state to a determined data state.

50. (Currently Amended) The ~~apparatus~~ testing circuit recited in claim 49, wherein the TAP controller is one of a plurality of controllers in a boundary scan chain.

51. (Currently Amended) The ~~apparatus~~ testing circuit recited in claim 49, wherein the second ~~circuit~~ logic begins transitioning the TAP controller from the undetermined data state to the determined data state when the TAP controller has reached an UPDATE-DR state.

52. (Currently Amended) The ~~apparatus~~ testing circuit recited in claim 51, wherein the TAP controller is one of a plurality of controllers in a boundary scan chain.